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Water-Induced Scandium Oxide Dielectric for Low-Operating Voltage n- and p-Type Metal-Oxide Thin-Film Transistors

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Solution-processed metal-oxide thin films based on high dielectric constant (*k*) materials have been extensively studied for use in low-cost and high-performance thin-film transistors (TFTs). Here, scandium oxide (ScO_x) is fabricated as a TFT dielectric with excellent electrical properties using a novel water-inducement method. The thin films are annealed at various temperatures and characterized by using X-ray diffraction, atomic-force microscopy, X-ray photoelectron spectroscopy, optical spectroscopy, and a series of electrical measurements. The optimized ScO_x thin film exhibits a low-leakage current density of 0.2 nA cm^{-2} at 2 MV cm^{-1}, a large areal capacitance of 460 nF cm^{-2} at 20 Hz and a permittivity of 12.1. To verify the possible applications of ScO_x thin films as the gate dielectric in complementary metal oxide semiconductor (CMOS) electronics, they were integrated in both n-type InZnO (IZO) and p-type CuO TFTs for testing. The water-induced full oxide IZO/ScO_x TFTs exhibit an excellent performance, including a high electron mobility of 27.7 cm^2 V^{-1} s^{-1}, a large current ratio (I_{on}/I_{off}) of 2.7 × 10^7 and high stability. Moreover, as far as we know it is the first time that solution-processed p-type oxide TFTs based on a high-*k* dielectric are achieved. The as-fabricated p-type CuO/ScO_x TFTs exhibit a large I_{on}/I_{off} of around 10^5 and a hole mobility of 0.8 cm^2 V^{-1} at an operating voltage of 3 V. To the best of our knowledge, these electrical parameters are among the highest performances for solution-processed p-type TFTs, which represents a great step towards the achievement of low-cost, all-oxide, and low-power consumption CMOS logics.

1. Introduction

In the past decade amorphous metal-oxide thin-film transistors (TFTs) have been studied in depth for applications in active-matrix organic light-emitting diodes (AMOLEDs), solar cells, biosensor arrays, and photodetectors.[1] Along with the rapid developments in display technology, high-resolution and high-speed displays have become one of the growing trends. In this regard, energy consumption has turned out to be an inevitable issue especially for mobile, battery-powered applications. As a low-voltage operation of the oxide TFTs is demanded for practical applications, it is necessary to develop novel gate dielectrics for producing a large areal capacitance.[2] The achievements of low-voltage oxide TFTs have been extensively reported in recent works, including the use of inorganic high-*k* dielectrics,[3] organic self-assembled-monolayer dielectrics,[4] and electrolyte dielectrics.[5] Among these, the use of inorganic high-*k* dielectrics is the most attractive option as it simultaneously enables a low leakage current, through the use of a thicker film, as well as a low-voltage operation. The high-*k* dielectrics can be prepared by various methods such as metal anodic oxidation method,[6] vacuum-based deposition,[7] and low-cost solution-based techniques.[8] To date, there are numerous candidate materials (e.g., Ta_2O_5,[7b] Y_2O_3,[7a,9] Al_2O_3,[10] ZrO_2,[2,11] HfO_2,[8a] $LaAlO_3$,[8b] HfON,[12] silicates,[13] etc.) that could potentially replace conventional dielectrics, such as SiO_2 and SiN_x. To the best of our knowledge, there are few reports on the demonstration of scandium oxide (Sc_2O_3) as the gate dielectric in TFT devices.

As a high-*k* material Sc_2O_3 has a dielectric constant of 14, a bandgap of 6.3 eV and an excellent thermal stability with Si.[14] In addition, Sc_2O_3 has been found to possess a negative fixed charge. This is beneficial to obtain a positive threshold or turn-on voltage for n-type TFTs that operate in the enhancement mode.[15]

Concerning the CMOS architecture development based on solution processing, a wet step is inevitably involved. In this regard, the resistance to moisture absorption is another important

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issue for the selection of the high-k dielectric material.[16] La_2O_3 has been previously regarded as a promising dielectric material because of its large band offset of 2.3 eV and high dielectric constant of 30.[3b] Unfortunately, the high moisture absorption of La_2O_3 limits its practical application in CMOS processes. Zhao et al. have proved that the moisture absorption in high-k oxides transforms metal oxides (M_mO_n) into metal hydroxides ($M(OH)_n$).[17] The moisture absorption speed is strongly related to the change in Gibbs free energy, ΔG, during the reaction. Here, a negative ΔG means a decrease in the system energy after the reaction, indicating the occurrence of transformation reactions. According to the ΔG calculation, only two high-k materials (Sc_2O_3 and HfO_2) showed positive ΔG values, indicating a high resistance to moisture absorption, and thus not the occurrence of a transformation reaction. It is well known that the first and commonly used high-k gate dielectric in commercial production is a Hf-based oxide material.[8a] As an alternative to that we propose Sc_2O_3 as an excellent dielectric candidate for further development of high-performance, low processing costs, and low power consumption CMOS logics.[18]

To date, Sc_2O_3 thin films have been prepared by using various costly vacuum-based techniques, such as molecular-beam epitaxy,[14b] chemical vapor deposition,[14a,19] electron-beam evaporation,[20] and high-pressure sputtering.[14c] In contrast, solution processing usually exhibits benefits such as simplicity, atmospheric processing, high throughput, large-area uniformity, roll-to-roll capability, and low fabrication cost.[21] However, solution-processed metal oxide thin films are usually fabricated from metal-organic precursors that contain large amounts of organic species. The thermal decomposition of these organic species tend to lead to disruptive volume changes, rough surfaces, and highly porous films.[22] In our recent report a water-inducement method was used for the first time to fabricate metal-oxide thin films and integrate these as channel layer in TFT devices.[23] This water-inducement route allows the preparation of precursor solutes in water without additional additives and catalysts. Therefore, the decomposition and densification of the oxide films can be achieved at lower annealing temperatures (T_a) compared to that of commonly used organic-based precursors. Moreover, the surface morphology of the annealed films is smoother due to the release and decomposition of small nitrate groups. Apart from that, the water-inducement method is simple and non-toxic and so has all the expected characteristics to substitute the commonly used organic-based synthetic approaches to fabricate full metal oxide based devices for the next generation of low cost and functional electronics.

In previous reports on solution-processed TFTs the channel layers were mostly composed of n-type metal oxides, which prevent the implementation of the complementary logic-based circuits with oxide TFTs. This is mainly related to the lack of p-type oxide semiconductors and the difficulty in growing high-quality film via a low-temperature process.[24] Recently, several groups have carried out research on exploring solution-processed p-type oxide TFTs. Kim et al.[25] demonstrated a spin-coated Cu_2O TFT at 700 °C with a field-effect mobility (μ_{FE}) of 0.16 $cm^2\ V^{-1}\ s^{-1}$ and an on/off current ratio (I_{on}/I_{off}) of 10^2. Anthopoulos's group[26] produced Cu_2O thin films by spray pyrolysis at a maximum temperature of 275 °C for 12 h and the as-fabricated Cu_2O TFTs exhibited an average μ_{FE} of 3×10^{-4} $cm^2\ V^{-1}\ s^{-1}$. Solution-processed p-type SnO TFTs were achieved by Okamura and co-workers,[27] exhibiting a μ_{FE} of the order of 0.13 $cm^2\ V^{-1}\ s^{-1}$ and an I_{on}/I_{off} of 85. Garlapati et al.[28] fabricated a low-operating voltage CuO TFT based on a polymer electrolyte dielectric at 400 °C. The CuO TFT exhibited a μ_{FE} of 0.22 $cm^2\ V^{-1}\ s^{-1}$ and an I_{on}/I_{off} of 10^3 at a low operating voltage of 1.5 V. As can be seen, the production of p-type oxide TFTs via low-temperature solution processing is highly demanded for the development of next-generation, low-cost, all-oxide based CMOS logics.

To accomplish this demand, herein we report for the first time a solution processed, p-type, metal-oxide TFT that uses a dielectric high-k ScO_x thin film fabricated by a simple water-inducement route. The physical properties of the ScO_x thin films as a function of annealing condition were systematically investigated. To verify the potential of ScO_x thin films as the gate dielectric in CMOS logics, their applications in n-type and p-type metal oxide TFTs were evaluated. In particular, we noticed that the p-type CuO/ScO_x TFT exhibited a high performance under a low operating voltage of 3 V, with a high I_{on}/I_{off} of around 10^5, and a hole mobility of ca. 0.8 $cm^2\ V^{-1}\ s^{-1}$.

2. Results and Discussion

2.1. Characterization of Water-Induced (WI) ScO_x Precursor

The thermal behavior of the WI ScO_x xerogel was investigated by thermogravimetic analysis (TGA) and the results are shown in **Figure 1**. The weight loss starting at around 100 °C is due to the evaporation of water, which was used as the solvent in the WI precursor solution. The molecules were drawn together during the evaporation of the solvent, which led to the transition from the 'sol' to the 'gel' state.[29] The subsequent weight loss can be attributed to the thermal decomposition of metal nitrate and the evaporation of the volatile nitrate precursor.[30] The dehydroxylation of the scandium hydroxide precursor occurred at around 260 °C and was completed at around 450 °C. No apparent weight loss was observed at temperatures above 450 °C, implying a complete conversion from the xerogel into scandium oxide.

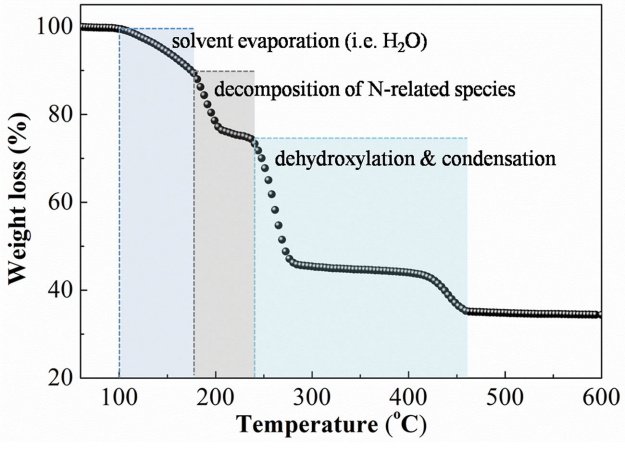

Figure 1. Thermal behavior of the WI ScO_x xerogel.

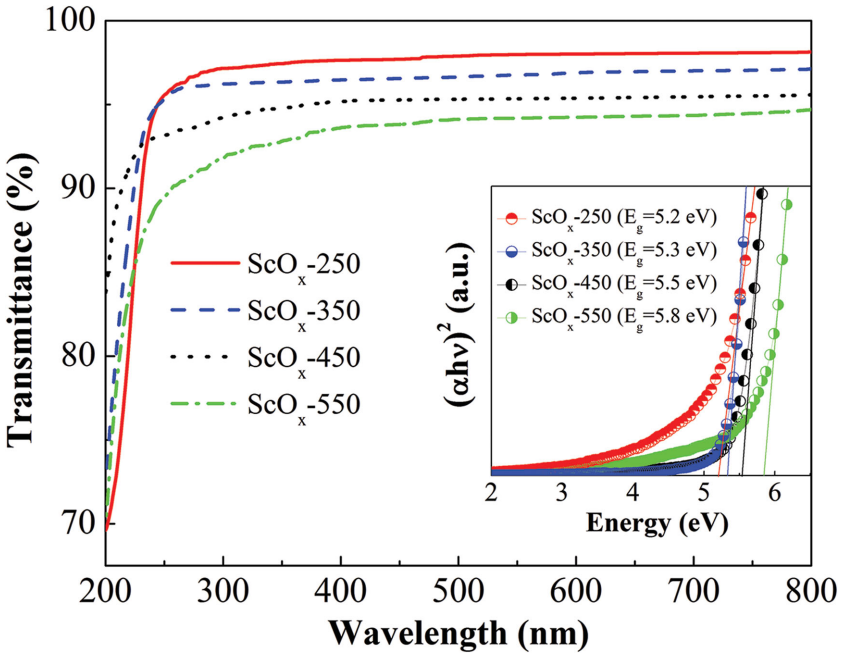

Figure 2. Optical transmittances of ScO_x dielectric thin films annealed at different temperatures. The inset shows the Tauc plots of the corresponding ScO_x thin films.

2.2. Optical Properties of WI ScO_x Thin Films

The novel fabricated WI ScO_x thin films were characterized by UV–vis transmittance measurements. All thin films exhibited average transmittances of over 94% in the visible range. Moreover, we noticed that the transmittance of the ScO_x thin films decreased as T_a increased. This decrease can be attributed to the slight increase in surface roughness or the elimination of interstitial oxygen at high annealing temperatures.[31] The optical bandgap (E_g) was calculated using a standard Tauc plot method[32] and the results are shown in the inset of **Figure 2**. The E_g value increased from 5.2 to 5.8 eV as T_a was enhanced from 250 to 550 °C. Larger E_g values make it possible to inhibit the carrier conduction between the channel layer and the dielectric layer. For the low-temperature-processed ScO_x thin film, the presence of defects in the thin film would produce localized states in the bandgap, which decreases the bandgap energy of the thin film. At high T_a, the annihilation of oxygen vacancies/defects results in a decrease of the density of states in the band structure, which leads to an increase of the bandgap energy of the ScO_x thin films.[33]

2.3. Surface Morphologies and Structural Properties of WI ScO_x Thin Films

It is well known that for high-performance TFTs it is critical to have a dielectric layer with a smooth surface as the carrier transport is highly influenced by the interface between the channel and the dielectric layers. The atomic force microscopy (AFM) images of the ScO_x thin films as a function of T_a are shown in **Figure 3**. The root mean square (RMS) values were 0.17, 0.17, 0.23, and 0.57 nm for ScO_x-250, ScO_x-350, ScO_x-450, and ScO_x-550, respectively. The surfaces were found to be quite smooth for the solution-processed dielectric layers with small RMS values (<1 nm).[3a,34] The smooth surfaces of the ScO_x thin films are not only related to their amorphous nature (Figure S1 in the Supporting Information), but also to the use of an organic-species-free WI precursor solution. In previous reports these types of solution-processed high-k dielectrics were generally prepared from organic-solvent-based precursor solutions.[3a,8a] During the post-annealing process, for instance, pyrolysis, the present organic ligands tend to release a large amount of volatile gases, which generate nanopores in the dielectric thin films. This will reduce the film density and increase the surface roughness and leakage current.[35] This is a bottleneck for the production of high-performance electronic devices.

2.4. Analysis of XPS Results for WI ScO_x Thin Films

The chemical compositions of WI ScO_x thin films were explored by XPS measurements. The O 1s binding energies of the ScO_x thin films fabricated at various temperatures are shown in **Figure 4**a. The binding energies of the O 1s peaks were deconvoluted into two peaks centered at 531.6 eV and 529.6 eV. The peaks centered at 529.6 eV and 531.6 eV can be assigned to the O^{2-} in ScO_x and the bonded oxygen, respectively, whereby the latter could be an oxygen vacancy, hydroxyl group, or absorbed H_2O on the film surface . For convenience, O_I/O_{total} and O_{II}/O_{total} are defined as the relative quantity of O^{2-} in ScO_x and the bonded oxygen in the ScO_x thin films, respectively. The ratios of O_I/O_{total} and O_{II}/O_{total} are summarized in Figure 4b. We found that with increasing T_a from 250 °C to 550 °C, the fraction of O^{2-} in ScO_x increases from 28.2% to 69.3%. The XPS results reveal that the bonded oxygen ions are removed and M-O bonds are created during the oxidation of the ScO_x thin films. Therefore, to be used as a good dielectric layer, the amount of bonded oxygen in the film should be kept at a relatively low level because the bonded oxygen generally creates defect states in the forbidden band of ScO_x, which will induce a leakage current and will lower the breakdown electric field.

Figure 4c exhibits the XPS Sc 2p spectra of ScO_x dielectrics annealed at various temperatures. All samples show the typical Sc 2p spectra with spin–orbit doublets ($p_{3/2}$ and $p_{1/2}$) separated by 4.4 eV, which indicates the formation of ScO_x. The atomic ratios (Sc/O) for ScO_x-250, ScO_x-350, ScO_x-450, and ScO_x-550 were calculated to be 1:3, 1:2.2, 1:2, and 1:1.9, respectively. As T_a was increased, both Sc 2p peaks shifted to lower binding energies. A similar phenomenon was reported previously[10a,36] for solution-processed ZrO_x and AlO_x films. The reasons for this shift can mainly be attributed to the progressive oxidization of ScO_x or to the decrease in the coordination number of M^{n+} ions in the film.

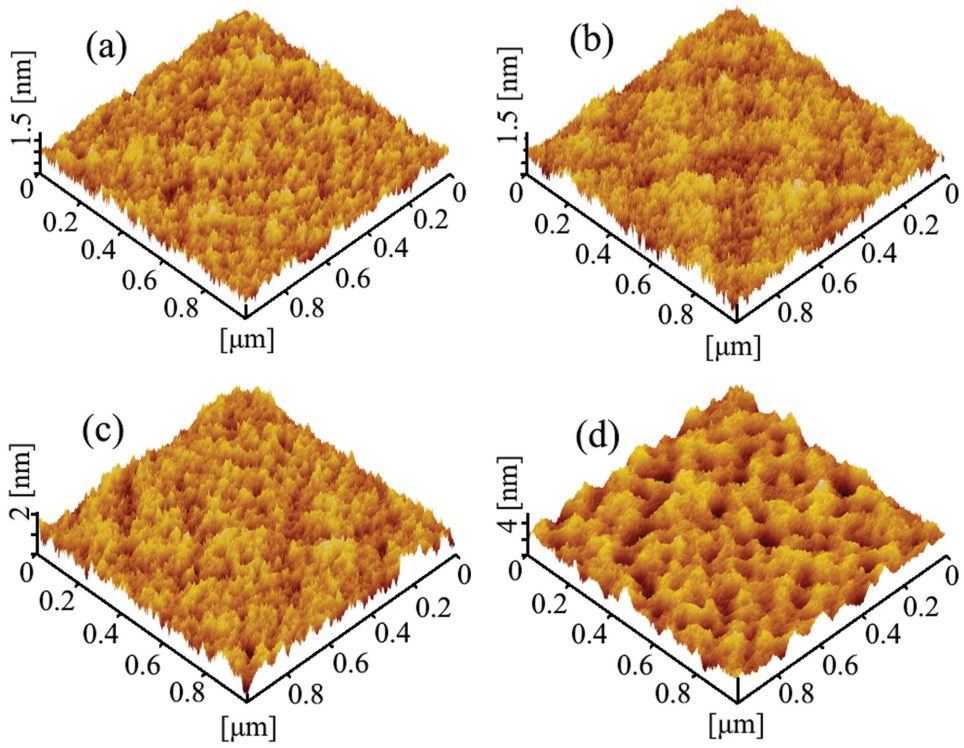

Figure 3. Surface morphologies of a) ScO_x-250, b) ScO_x-350, c) ScO_x-450, and d) ScO_x-550.

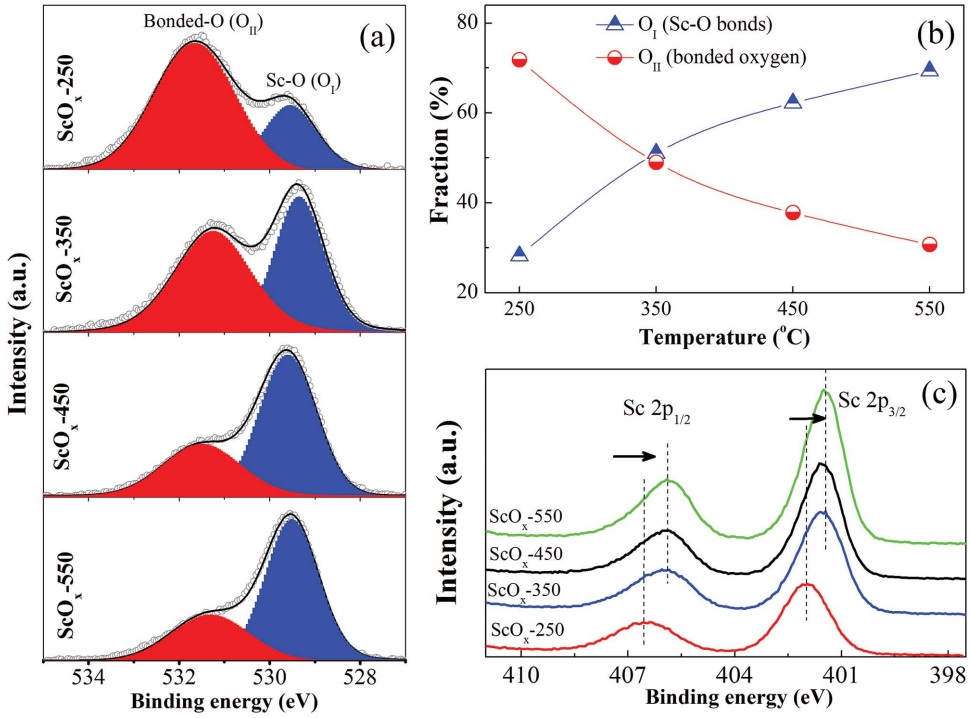

Figure 4. a) XPS spectra of O 1s peaks for ScO_x dielectrics as a function of T_a. b) The variation of oxygen components at various annealing temperatures. c) The corresponding XPS Sc 2p spectra of the ScO_x thin films.

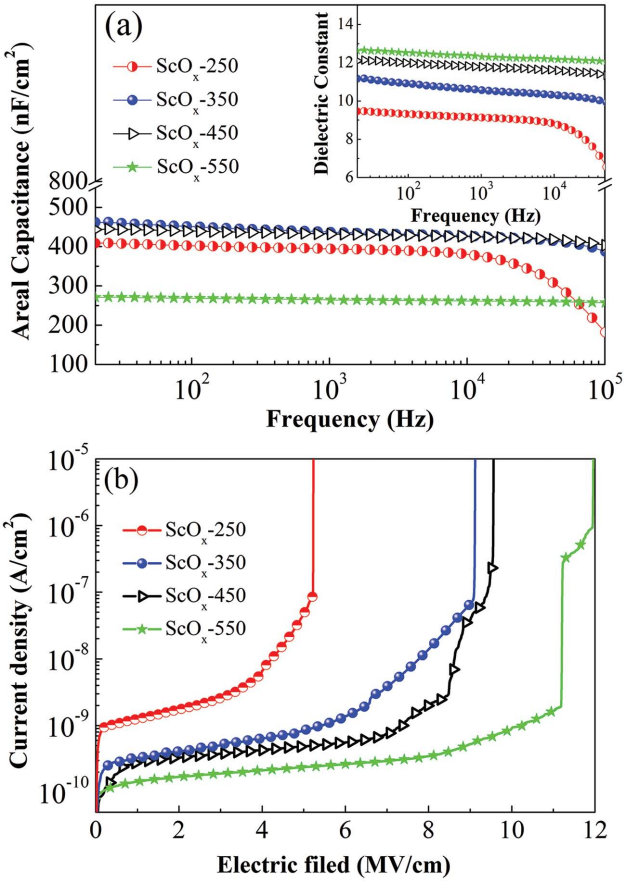

Figure 5. Variation of a) the *C*–*f* and b) J_{leak}–*E* characteristics for Al/ScO$_x$/p$^+$-Si capacitors.

2.5. Dielectric and Electrical Properties of WI ScO$_x$ Dielectric

To investigate the dielectric and electrical properties of the WI ScO$_x$ thin films annealed at various temperatures, capacitors with a structure of Al/ScO$_x$/p$^+$-Si were used. **Figure 5**a shows the areal capacitance (*C*) as a function of frequency (*f*) for ScO$_x$ capacitors. The corresponding dielectric constant dispersions are shown in the inset of Figure 5a. The capacitance densities at 20 Hz were found to be 408, 460, 450, and 270 nF cm^{-2} for ScO$_x$-250, ScO$_x$-350, ScO$_x$-450, and ScO$_x$-550, respectively. In the low-frequency region the areal capacitance increased as T_a increased from 250 to 350 °C and then decreased again for thin films annealed at temperatures higher than 350 °C. The reason for the increase of the capacitance for ScO$_x$-350 °C can be attributed to the thermally enhanced dehydroxylation once the capacitance of the metal hydroxide is smaller than that of the metal oxide.[9] When the T_a was higher than 350 °C most of the scandium hydroxide was converted into ScO$_x$. The decrease in the capacitance can be mainly attributed to the existence of a metal–silicate interface.[37] Assuming that the interfacial layer between Si and ScO$_x$ is mostly comprised of SiO$_2$, the measured ScO$_x$ capacitance corresponds to the combination of capacitors in series: $\frac{1}{C_{total}} = \frac{1}{C_{ScO_x}} + \frac{1}{C_{SiO_2}}$.

By introducing the *k* values and the thickness of the films, the decreased capacitance at higher annealing temperatures (>350 °C) can be well explained by the dominant role played by the SiO$_2$-like capacitor (details not shown here).

Figure 5b shows the leakage current density (J_{leak}) versus electric field (*E*) measurements carried out to evaluate the leakage behavior of the ScO$_x$ thin films. The relatively large J_{leak} for ScO$_x$-250 is mainly related to the defects associated with the residual nitrate and hydroxyl groups. The leakage current profiles were found to decrease in slope as T_a increased indicating a reduction in the electronic defects as the annealing temperature increased.[8b] The current density levels for ScO$_x$-350 and ScO$_x$-450 were similar (less than 0.3 nA cm^{-2} at 2 MV cm^{-1}). Although the ScO$_x$-550 dielectric film had the lowest J_{leak} value, it also showed the smallest areal capacitance, which would undoubtedly limit its performance in electronic devices.

2.6. Solution-Processed n-Type IZO/ScO$_x$ TFTs

To verify the possible application of ScO$_x$ thin films as gate dielectrics, bottom-gated TFTs combined with a WI n-type IZO channel and p-type CuO channel were separately evaluated. In this study ScO$_x$-350 was selected as the best dielectric layer because of its relatively low J_{leak} and large capacitance. Moreover, temperatures lower than 350 °C are generally needed to employ a solution process in practical fabrication processes for flat-panel displays.[38] For the WI n-type IZO/ScO$_x$ TFT, the typical output and transfer curves are shown in **Figure 6**a,b. The IZO/ScO$_x$ TFT shows a high electrical performance, such as a high μ_{FE} of 27.7 cm^2 V^{-1} s^{-1}, an I_{on}/I_{off} of around 10^7, a small *SS* value of 100 mV dec^{-1}, a turn-on voltage (V_{on}) close to 0 V, and a hysteresis of about 0.06 V. Here, we would like to emphasize that these as-fabricated TFTs can be operated at an ultra-low voltage of 1.5 V, which is 20 times lower than that for conventional SiO$_2$-based TFTs (Figure S2, Supporting Information). This is because of the high *k* value and the small thickness of the ScO$_x$ dielectric. The negligible hysteresis observed indicates that there are small amounts of bulk traps within the IZO channel layer and interface traps between the ScO$_x$ dielectric and the IZO channel layer. The maximum areal density of states $\left(N_s^{max}\right)$ calculated from the *SS* value (see Experimental Section) was 3 × 10^{12} cm^{-2} for the IZO/ScO$_x$ TFT. Such an N_s^{max} value is quite acceptable compared to previously reported TFTs based on solution-processed high-*k* dielectrics, such as YO$_x$ (2.7 × 10^{12} cm^{-2}),[9] AlO$_x$ (1.1 × 10^{12} cm^{-2}), ZrO$_x$ (7.6 × 10^{12} cm^{-2}),[3a] and HfO$_x$/AlO$_x$ (1.6 × 10^{12} cm^{-2}).[39] Thus, the small N_s^{max} obtained indicates that the ScO$_x$ thin films are highly attractive as dielectric to produce TFTs with excellent electrical performances, once the channel/dielectric interface is highly improved, from which the carrier transport in the interface region benefits as well as the overall device operational stability.

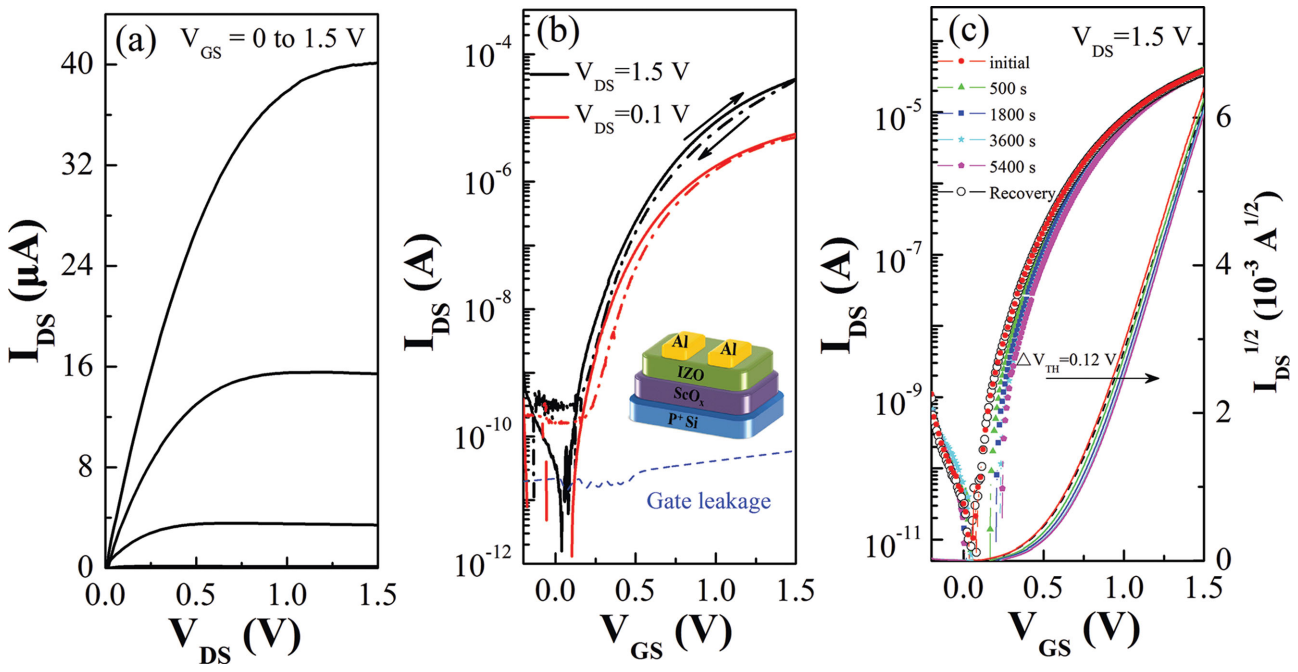

Figure 6. a) Output and b) transfer characteristics of the IZO/ScO_x TFT. c) Transfer characteristics of the IZO/ScO_x TFT with a V_G of 1.5 V for 5400 s and its recovery behavior.

Although oxide TFTs based on a high-*k* dielectric obtained via a low-temperature solution process have been previously realized, to the best of our knowledge there has been no reports to demonstrate their electrical stability under long-term bias stressing. To investigate the bias stability of the WI IZO/ScO_x TFT positive bias stress (PBS) tests were performed by applying a constant gate bias of 1.5 V whereby the source and drain electrodes were grounded. The device was stressed for 5400 s and allowed to recover in the dark. The results are shown in Figure 6c. The TFT exhibited an acceptable operational stability with a small threshold voltage shift (ΔV_{TH}) of 0.12 V, which returned to its original position after 120 min. The negligible change in the *SS* value reveals that there is no additional defect creation at the channel/dielectric interface during bias stressing. The small ΔV_{TH} shift value reveals that there are a small number of defects at the IZO/ScO_x interface, which is consistent with the N_s^{max} data.

In this work, an areal capacitance of 460 nF cm^{-2} was obtained at a frequency of 20 Hz to avoid mobility overestimation.[40] It should be noted that by replacing SiO_2 with the high-*k* ScO_x dielectric, the μ_{FE} was significantly enhanced by a factor of 9. This increase in μ_{FE} benefits from both the electronically clean interface and the high capacitance density of the ScO_x dielectric. In the oxide semiconductors, the carrier transport is governed by dense localized states within the forbidden bandgap, although the overlapping of the spherical *s*-orbitals provides an efficient transport path.[41] The electron transport in the amorphous n-type IZO channel layer is dominated by electron hopping between neighboring cation ions (**Figure 7**a). Before participating in the conducting transport, the induced electrons have to fill the localized states between the energy gaps (Figure 7b). In the TFTs with an identical device structure, the amount of charge carriers induced by the external electric field are proportional to the capacitance of the gate insulator. Therefore, when the high-*k* ScO_x films were used as the gate dielectric, a large amount of attracted electrons quickly filled the lower-lying localized states in the oxide semiconductors. Then, the additionally accumulated electrons could occupy the upper-lying localized states. As a result, the electrons could jump to the neighboring localized states easily, along the percolating–conduction path, which resulted in an enhanced electron mobility.

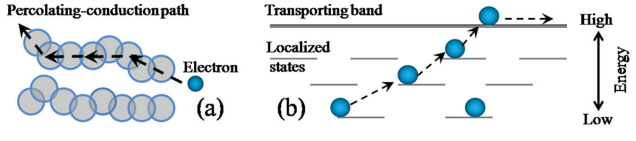

Figure 7. a) Schematic of electron-transporting mode and b) energy-band diagram in n-type amorphous oxide semiconductors.

2.7. Solution-Processed p-Type CuO/ScO_x TFTs

After the successful fabrication of high-performance n-type IZO TFTs based on high-*k* ScO_x dielectric, we also attempted to demonstrate the feasibility of solution-processed p-type TFTs based on the ScO_x dielectric layer. As previously mentioned, previously reported solution-processed p-type oxide TFTs exhibited low electrical performances, which significantly limited the development of fully-oxide low-power consumption CMOS logics. In order to prepare high-quality p-type oxide films, the most straightforward way is to control the oxidation of the metallic layer.[26,42] In this work a polyol reduction method was adopted to synthesize the metallic layer because of its low-temperature process possibilities and electrical characteristics.[43]

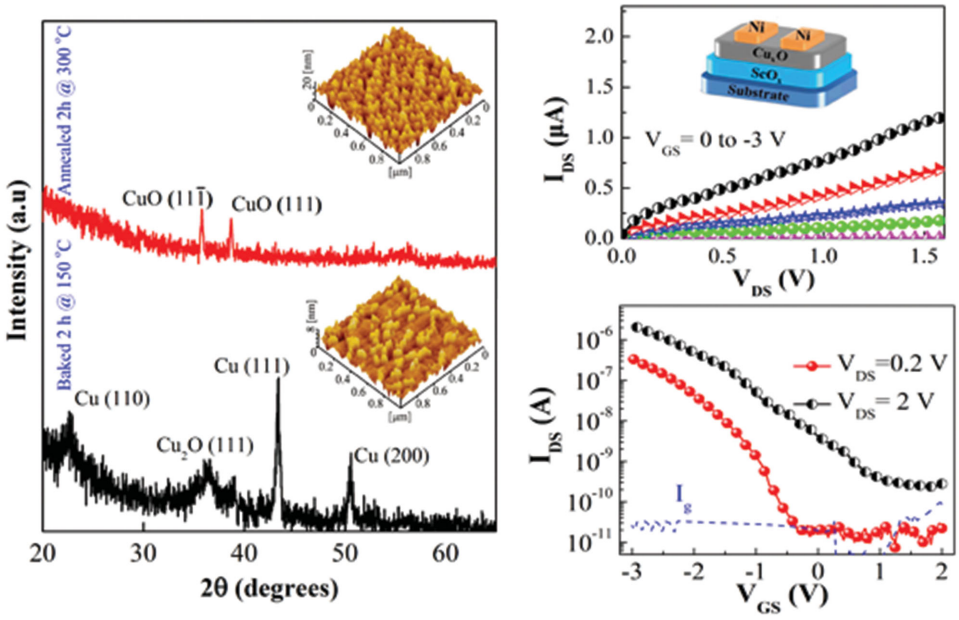

Figure 8. a) XRD patterns of the CuO thin film annealed at 150 °C and 300 °C in air for 2 h. The insets show the AFM images of the corresponding films. b) Output and c) transfer characteristics of the CuO/ScO_x TFT under different V_{DS}. Here, the dotted line corresponds to the off current (I_{off})

Polyalcohols, such as ethylene glycol and glycerol, hereby act as the solvent as well as the mild reducing agent.

In this work copper oxide (CuO), known to be a typical p-type oxide material, was used as the TFT channel layer and was incorporated in TFTs with a ScO_x dielectric. As shown in **Figure 8**a, the CuO gel was decomposed into metallic copper at a low temperature of 150 °C. The 300 °C-annealed CuO film, used as the TFT channel, consisted of a mixture of CuO (11$\bar{1}$) and CuO (111). The surface morphologies revealed that the CuO film that was annealed at 300 °C had a uniform surface (RMS = 3.9 nm) with an average grain size of 40 nm. It is well known that the electrical performance of the TFTs strongly depends on the surface roughness and the crystalline structure of the thin films.[25] Thus, films with smooth surfaces and large grain sizes lead to less grain boundaries, which is beneficial to improve the hole mobility and the reliability of the TFTs.

The output and transfer characteristics of the p-type CuO/ScO_x TFTs are shown in Figure 8b,c. CuO TFTs based on a SiO_2 dielectric were also fabricated for comparison. The key electrical parameters of the TFT devices are summarized in **Table 1**. Note that the I_{DS} monotonically increases as the gate voltage V_{GS} is reduced from 0 to −3 V, which is a typical characteristic of a TFT with a p-type channel. The non-ideal current saturation behavior in the output curves can be due to two main reasons. The first one is related to a poor CuO film quality, which can be caused by the agglomeration of the CuO nanopowders.[5b] The second reason is related to the relatively high hole concentration in the CuO channel layer.[44] Overall, the p-type device exhibits promising operating characteristics with large I_{on}/I_{off} values (~10^5) and a hole mobility of around 0.8 cm^2 V^{-1} s^{-1}. The hole mobility achieved in this report is much larger than previously reported values regarding solution-processed Cu-based oxides as channel layers (in the range of 0.001 to 0.22 cm^2 V^{-1} s^{-1}).[25–28] The improved features are undoubtedly related to the high-k ScO_x dielectric, high-quality CuO channel layer, and the electronically clean interface of CuO/ScO_x, which can be concluded by comparing these results to the ones achieved using a CuO/SiO_2 system, as shown in Table 1.

Table 1. Electrical parameters of the n-type IZO and p-type CuO TFT based on SiO_2 and ScO_x dielectrics.[a)]

TFT structure	μ_{FE} [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	V_{TH} [V]	SS [V dec^{-1}]
IZO/SiO_2	3.35 ± 0.25	~10^8	1.50 ± 0.20	0.5 ± 0.02
IZO/ScO_x	27.71 ± 1.15	~10^7	0.52 ± 0.04	~0.1
CuO/SiO_2	0.26 ± 0.04	10^5–10^6	−8.2 ± 0.50	1.9 ± 0.10
CuO/ScO_x	0.78 ± 0.03	~10^5	−0.6 ± 0.05	~0.4

[a)]Each device metric is the average of 12 devices (3 × 4 array).

In recent reports of solution-processed TFTs, high-mobility-driven studies that were carried out suffered from small I_{on}/I_{off} and large I_{off} values (>10^{-9} A).[10a,40,45] The large I_{off} value undoubtedly results in more power dissipation, and yields unstable and unreliable TFTs. In those reports, the high-k dielectrics were prepared using organic-based precursor solutions. During the post-annealing process, the pyrolysis of organic ligands tends to release a large amount of volatile gases, which would generate nanopores in the resultant dielectric films. This in turn is problematic for high-performance electronic devices. However, in this report, the organic-free WI precursor solution can effectively reduce the formation of volatile gases. In addition, the UV-assisted pre-treatment allows the moderation of the decomposition of the NO_3^- species in the gel film, which makes the surface roughness and surface energy small.[46] As a result, the TFTs based on high-quality ScO_x dielectrics exhibit high I_{on}/I_{off} values with a low I_{off} of around 10^{-11} A.

3. Conclusions

Novel ScO_x dielectric thin films were fabricated via a water-inducement route for the first time. Here, the precursor solution for the preparation of the ScO_x thin films contained water and metal nitrates without additional organic additives and catalysts. The physical properties of the WI ScO_x films were characterized using different structural, morphological, composition, optical, and electrical techniques. The results showed that ScO_x thin films annealed at 250–550 °C exhibit a high transparency (>90%), smooth surface (<0.6 nm), and are amorphous. To verify the possible application of the ScO_x thin films as the gate dielectric in low-temperature-processed (≤350 °C) CMOS logics, n-type IZO and p-type CuO channel-based TFTs were integrated on the prepared ScO_x dielectric thin films. Both n- and p-type TFTs exhibited improved electrical performances at much lower operating voltages compared to those of SiO_2-based TFTs. In particular, the p-type CuO/ScO_x TFT exhibited a much higher electrical performance under a gate bias of 3 V, with an I_{on}/I_{off} value of around 10^5 and hole mobility of 0.8 $cm^2\ V^{-1}\ s^{-1}$. To the best of our knowledge, this is the first report on such high performances for solution-processed p-type oxide TFTs based on a high-*k* dielectric, which represents a great step towards the development of next-generation, low-cost, all-oxide CMOS electronics.

4. Experimental Section

Precursor Solution Preparation and Characterization: The WI ScO_x precursor solution (0.1 M) was prepared by dissolving $Sc(NO_3)_3{\bullet}6H_2O$ in deionized (DI) water. The 0.1 M IZO precursor solution was prepared by dissolving $In(NO_3)_3{\bullet}H_2O$ and $Zn(NO_3)_2{\bullet}H_2O$ in DI water. The molar ratio of In/Zn was 7:3. The CuO precursor solution with a concentration of 0.1 M was prepared by dissolving $Cu(NO_3)_2{\bullet}3H_2O$ in a mixture of DI water and glycerol. The method was reported somewhere else.[28] After that, these precursor solutions were stirred for 6 h before fabrication. The thermal behavior of the ScO_x xerogel was monitored under ambient air using a thermogravimetric analyzer (TGA, Pyris 1) at a heating rate of 10 °C min^{-1}.

Thin Film Fabrication and Characterization: Prior to thin-film fabrication, heavily doped p-type Si substrates were cleaned ultrasonically in acetone, ethanol, and then DI water and dried by N_2 gun. The ScO_x solution was filtered through a 0.22-μm polytetrafluoroethylene (PTFE) syringe filter and then spun on the hydrophilic Si substrates at 500 rpm for 5 s and 5000 rpm for 20 s. Before the thermal annealing process was carried out, the ScO_x samples were treated by UV-assisted irradiation for 30 min. For convenience, the ScO_x thin films annealed at 250, 350, 450, and 550 °C, hereafter, will be abbreviated as ScO_x-250, ScO_x-350, ScO_x-450, and ScO_x-550, respectively. The thicknesses of ScO_x-250, ScO_x-350, ScO_x-450, and ScO_x-550, measured by spectroscopic ellipsometry (ESS01, Sofn Instrument), were 28, 23, 23, and 25 nm, respectively. The transmittances of ScO_x films on sapphire were analyzed by UV–vis spectroscopy (UV-2550, Shimadzu). The crystal structures of ScO_x and Cu_xO thin films were investigated by X-ray diffractometry (XRD, X'Pert-PRO, PANalytical, Holland) with CuKα1 radiation. The surface morphologies of ScO_x and Cu_xO films were measured by using an atomic force microscope (AFM, SPA-400, Seiko). The chemical compositions of the ScO_x films were analyzed by X-ray photoelectron spectroscopy (XPS, ESCALAB 250).

Electronic Device Fabrication and Characteristics: To fabricate the WI n-type IZO TFTs based on the ScO_x dielectric, the IZO precursor was spin-coated on the ScO_x-350 dielectric at 5000 rpm for 25 s. The laminated samples were subsequently annealed at 300 °C for 120 min. After that, the Al source and drain electrodes were evaporated on the IZO channel layer through a shadow mask. To fabricate the p-type CuO TFTs based on the ScO_x dielectric layer, the CuO precursor solution was spin-coated on the ScO_x-350 dielectric at 5000 rpm for 25 s. The laminated samples were subsequently annealed at 300 °C for 120 min. The Ni source and drain electrodes were then evaporated on CuO channel layer through a shadow mask. In this report, the channel length and width of the TFTs were 250 and 1000 μm, respectively. For comparison, the n-type IZO and p-type CuO TFTs based on a thermally grown SiO_2 (100 nm) dielectric layer were also fabricated, which were used as reference devices. To examine the dielectric properties of the ScO_x thin films, capacitors with a structure of Al/ScO_x/p^+-Si were fabricated and investigated using an impedance analyzer (4294A, Agilent). The electrical properties of the ScO_x capacitors and the integrated TFT devices were measured under ambient conditions using a semiconductor parameter analyzer (Keithley 2634B) in a dark box. The field-effect mobility (μ_{FE}) was extracted from the transfer characteristics using:[1]

$$I_{DS} = \left(\frac{W}{2L} C_i \mu_{FE}\right)\left(V_G - V_{TH}\right)^2 \quad (1)$$

where C_i is the areal capacitance of the dielectric; W and L are the channel width and length of the TFT, respectively; V_G is the gate voltage and V_{TH} is the threshold voltage, which can be determined in the saturation region by the linear fitting of the $I_D^{1/2}$ vs. V_G plot. The maximum areal density of states (N_s^{max}) of the TFT device was calculated using:[47]

$$SS = \frac{\kappa T \ln 10}{e}\left[1 + \frac{e^2}{c_i} N_s^{max}\right] \quad (2)$$

where k is the Boltzmann constant, e is the electron charge, SS is the subthreshold swing of the transfer curve.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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